JY5312/5315

Simultaneous Data Acquisition Modules

User Manual

User Manual Version: V1.5.5

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Table of Contents

1. Overview

This chapter presents the information how to use this manual and quick start if you are already familiar with Microsoft Visual Studio and C# programming language.

1.1 Introduction

JY5312/5315 Series Simultaneous DAQ provide 16-channel, 16 bits resolution, up to 5M samples per second per channel. It also has 16 digital IO lines. JY5312/5315 can be run on PCIe, PXIe, TXI(Thunderbolt) and USB bus (coming soon) platforms. Depending on the model number, a JY5312/5315 series provide different sampling rate as shown in Table 1.

531x Model	AI Channels	Sample Rate (MS/s)	AI Resolution	DIO+PFI
5312	16	2	16	16
5315	16	5	16	16

Table 1 JY5312/5315 Family and Main Features

531x Model	PCIe	PXIe	TXI	USB
5312	√	√	√	√
5315	√	√	√	√

Table 2 JY5312/5315 on Different Bus

1.2 Main Features

- 16 simultaneous anlog input channels
- Maximun sample rate : 5 MS/ per channel
- 16 bits resolution
- 4 voltage ranges: ±10 V / ±5 V / ±2 V / ±1 V
- 256M samples of FIFO buffer
- 8 ports digital IO, 2 channels per port
- Analog/Digital/Software Trigger

1.3 Abbreviations

AI: Analog Input
DI: Digital Input
DO: Digital Output
DAQ: Data AcQuisition
ADC: Analog-to-Digital Conversion
PFI: Programmable Function Interface
DIFF: Differential

1.4 Learn by example

JYTEK has added **Learn by Example** in this manual. We provide many sample programs for this device. Please download and install the sample programs for this device. You can visit our web www.jytek.com to search for the example file or you can download a JYPEDIA excel file from our web. Open JYPEDIA and search for JYJY5312/5315 in the driver sheet, select the latest **JYJY5312/5315 Examples.zip**. This will lead you to download the sample program for this device. In addition to the download information, JYPEDIA also has a lot of other valuable information, JYTEK highly recommend you use this file to obtain information from JYTEK.

Figure 1 JYPEDIA Information

In a **Learn by Example** section, the sample program is in bold style such as **Analog Input-->Winform AI Continuous MultiChannel Soft Trigger**; the property name in the sample program is also in bold style such as **SamplesToAcquire**; the technical names used in the manual is in italic style such as *SampleRate*. You can easily relate the property names in the example program with the manual documentation.

In an **Learn by Example 5.2~5.5** section, the experiment is set up as follow. The JYJY5312/5315 is connected to a TB-68 terminal block. A signal source is also connected to the same terminal block as shown Figure 2.

Figure 2 Experiment Setup

The TB-68 is shown below as Table 3. In the rest of this manual, the wire connection in each **Learn by Example** section will be given by the pin numbers only.

Connector 0			
Pin	**Signal Name**	**Pin**	**Signal Name**
1	PFI0 / P0.0	35	PFI1 / P0.1
2	PFI2 / P1.0	36	PFI3 / P1.1
3	PFI4 / P2.0	37	PFI5 / P2.1
4	PFI6 / P3.0	38	PFI7 / P3.1
5	DGND	39	DGND
6	PFI8 / P4.0	40	PFI9 / P4.1
7	PFI10 / P5.0	41	PFI11 / P5.1
8	PFI12 / P6.0	42	PFI13 / P6.1
9	PFI14 / P7.0	43	PFI15 / P7.1
10	DGND	44	DGND
11	AI7-	45	AI7+
12	AI_GND	46	AI_GND
13	AI15-	47	AI15+
14	AI6-	48	AI6+
15	AI_GND	49	AI_GND
16	AI14-	50	AI14+
17	AI5-	51	AI5+
18	AI_GND	52	AI_GND
19	AI13-	53	AI13+
20	AI4-	54	AI4+
21	AI_GND	55	AI_GND
22	AI12-	56	AI12+
23	AI3-	57	AI3+
24	AI_GND	58	AI_GND
25	AI11-	59	AI11+
26	AI2-	60	AI2+
27	AI_GND	61	AI_GND
28	AI10-	62	AI10+
29	AI1-	63	AI1+
30	AI_GND	64	AI_GND
31	AI9-	65	AI9+
32	AI0-	66	AI0+
33	AI_GND	67	AI_GND
34	AI8-	68	AI8+

Table 3 TB-68 Front Panel for JY5312/5315 Series

2. Hardware Specifications

2.1 Analog Input Specifications

Analog Input	5312	5315
Number of Input channels	16	
ADC resolution (Bits)	16	
Sampling Rate	2 M Sample/s	5 M Sample/s
Clock	200 MHz	
Input range(V)	±10/±5/±2/±1	
Maximum Working Voltage(V)	±10.83 V（ref. AIGND）	
Input Terminal Type	Differential	
Input impedance(AI+ vs AIGND)	5.3 GΩ || 50 pF	
Input impedance(AI- vs AIGND)	5.3 GΩ || 50 pF	
Input coupling	DC	
CMRR(@60 Hz)*[1]	105 dB	
Crosstalk(@100 KHz)[*1]	Adjacent Ch: -90 dB, Non-adjacent: -105 dB	
DNL	No Missing Code	
INL	30 ppm of range	
Input FIFO	256 M Samples	
Trigger Type	Analog/Digital/Software	
Analog Trigger Voltage Range	Software Programmable Between -10 V ~ +10 V	
Trigger Mode	StartTrigger,ReferenceTrigger,ReTrigger	
Interval of retrigger	5 Samples	
Bandwidth (-3 dB)[*2]	2.2 MHz	
Overvoltage protection	ON: ±25 V ; OFF: ±15 V	
Input current during overvoltage protection	±20 mA	
*1 ±1 Range Typical Test *2 ±10 Range Typical Test		

Table 4 Analog Input Specifications

2.2 AI Accuracy

Your measurement accuracy is calculated by following fomular:

$$Accuracy = \pm(\%\ of\ Reading + \%\ of\ Range)$$

For example at 5V range and 24 Hours column, if your measurement is 2V, the accuracy of this measurement is:

$$\pm(0.0023\% * 2 + 0.0153\% * 5) = \pm 0.000811\text{V} = \pm 811\text{uV}$$

You can also get a good estimate by looking up the full scale accuracy for each range.

JY531X Accuracy = ±(% of Reading+% of Range)

Nominal Range (V)	Sample Rate per Channel[1]	Resolution (16-bits) (uV)	24 Hour Tcal ±1°C[2]			90 Days Tcal ± 5°C[3]			Temperature Coefficients (/ °C)[4]			24 Hr Full Scale Accuracy	90 Days Full Scale Accuracy
10	5 MS/s, 2MS/s	305.2	0.0023	+	0.0153	0.0044	+	0.0158	0.0005	+	0.0001	1755 uV	2015 uV
5	5 MS/s, 2MS/s	152.6	0.0018	+	0.0156	0.0038	+	0.0162	0.0005	+	0.0001	872 uV	998 uV
2	5 MS/s, 2MS/s	61.0	0.0022	+	0.0182	0.0040	+	0.0196	0.0005	+	0.0004	407 uV	473 uV
1	5 MS/s, 2MS/s	30.5	0.0017	+	0.0222	0.0041	+	0.0253	0.0006	+	0.0008	239 uV	293 uV

1. Accuracies apply to Sample Rate 5 MS/s for 5315 or 2MS/s for 5312.
2. Add temperature error for each °C outside Tcal± 5°C , 1PPM=0.0001%.
3. Add 20% to Gain and Offset Errors From 91 Days to 1 Year. Priliminary.
4. Specs subject to minor changes when more tests become available.
5. Accuracy valid to ±9.5V only.

Tcal=23°C in this table.

Table 5 AI Accuracy

2.3 Temperature Coefficients

When the operating temperature is outside the last calibration temperature, the accuracies in the table need to be adjusted. For example, In Table 4, if the operating temperature is 3°C outside the last calibration temperature range, the temperature adjustment at 5V range will be 3*(0.0023% of reading + 0.0153% of range) = (0.0069% of reading + 0.0459% of range). This adjustment needs to be added to 24 Hour or 90 Days accuracy entries. In the case of the 24 Hour column, the accuracy entry becomes (0.0092% of reading + 0.0612% of range). The same 2V measurement now has the accuracy:

$$\pm(0.0092\% * 2 + 0.0612\% * 5) = \pm 0.003244\text{V} = \pm 3244\text{uV}$$

2.4 AI Bandwidth

Range (V)	-3dB Bandwidth （MHz）
10	2.2
5	2.1
2	2
1	1.6

Table 6 AI Bandwidth

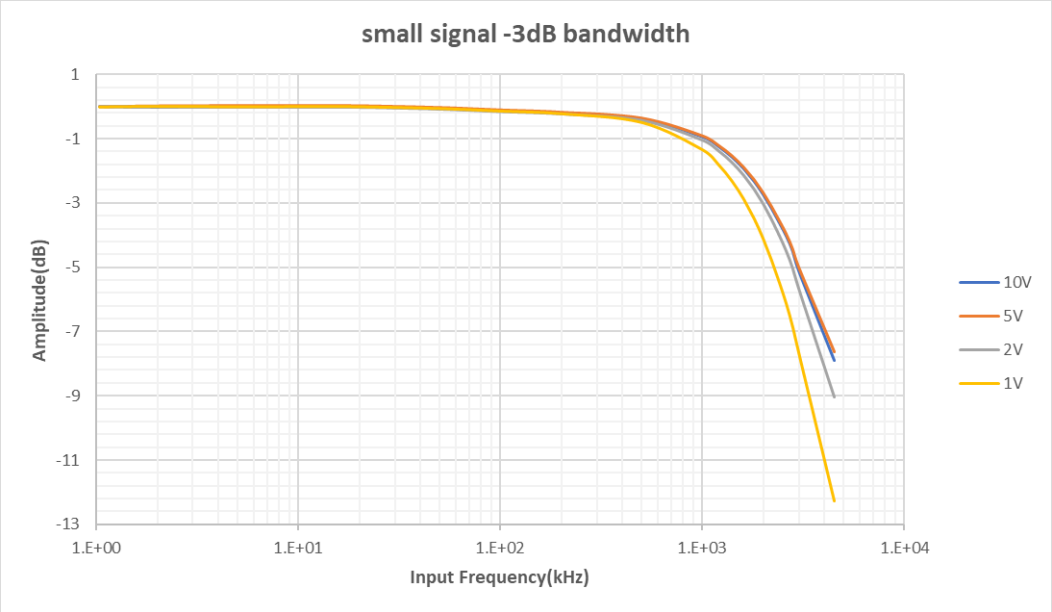

Figure 3 -3dB Bandwidth

2.5 CMRR

Range (V)	CMRR (dB at 60 Hz)
10	86.9
5	93.6
2	103.0
1	113.0

Table 7 CMRR

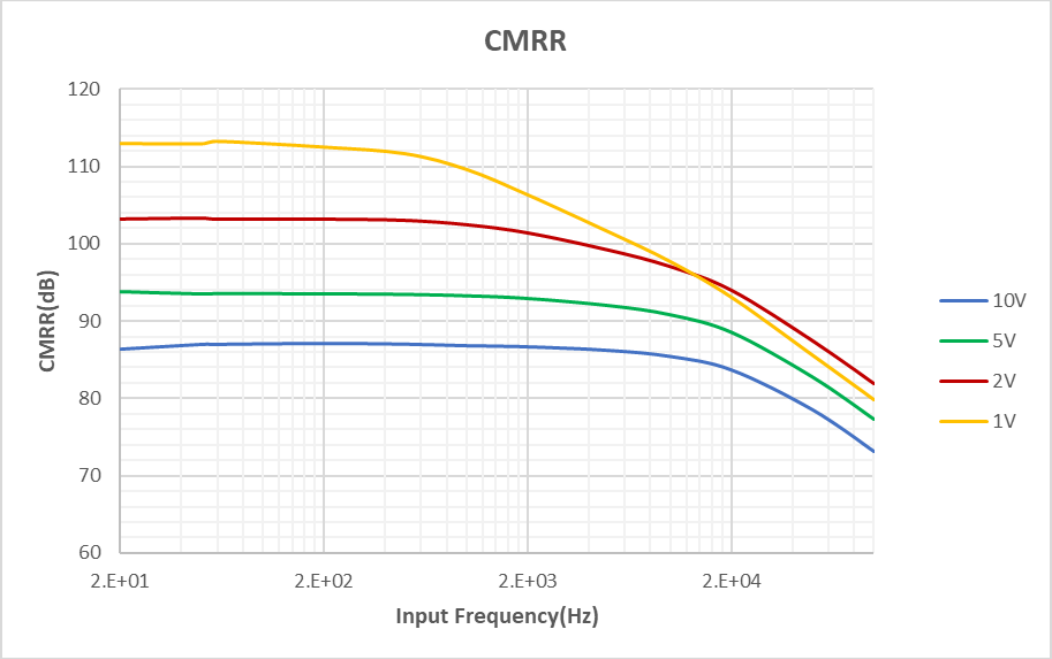

Figure 4 CMRR

2.6 Crosstalk

2.6.1 Adjacent channel

Range (V)	Crosstalk (dB at 100 kHz)
10	-113
5	-113
2	-113
1	-114

Table 8 Crosstalk (Adjacent channel)

2.6.2 Non-adjacent channel

Range (V)	Crosstalk (dB at 100 kHz)
10	-128
5	-127
2	-127
1	-126

Table 9 Crosstalk (Non-adjacent channel)

2.7 Digital IO Specifications

Number of channels	Port<0..7>
Ground reference	D GND
Directional control	Independent control of each port
Initial state	Input
Digital Input	Logic Low: V_{IL} Min : 0 V / Max : 1.0 V Logic High: V_{IH} Min : 2V / Max : 5.3V
Digital Output	Logic Low : 0 V, I_{OL} Max: 24 mA Logic High : 2.6 V～5 V, I_{OH}: -24 mA～0 mA
Overvoltage Protection	Continuous 30 mA -3.9 V～ 8.9 V; Instantaneous 200 mA -25 V～ 25 V; Duty cycle of instantaneous current pulse does not exceed 15%

Table 10 Digital IO Specifications

2.8 PFI Specifications

Number of channels	16
External digital trigger interface	Trigger voltage 3.3 V TTL; Trigger edge: Rising/Falling
Initial state	Input

Table 11 PFI Specifications

2.9 Power Specification

3.3V	2.13 A
12V	0.95 A

Table 12 Power Specification

2.10 Physical and Environment

Operating Environment

Ambient temperature range	0 °C to 50 °C
Relative humidity range	20% to 80%, noncondensing

Storage Environment

Ambient temperature range	-20 °C to 80 °C
Relative humidity range	10% to 90%, noncondensing

Table 13 Physical and Environment

2.11 Front Panel and Pin Definition

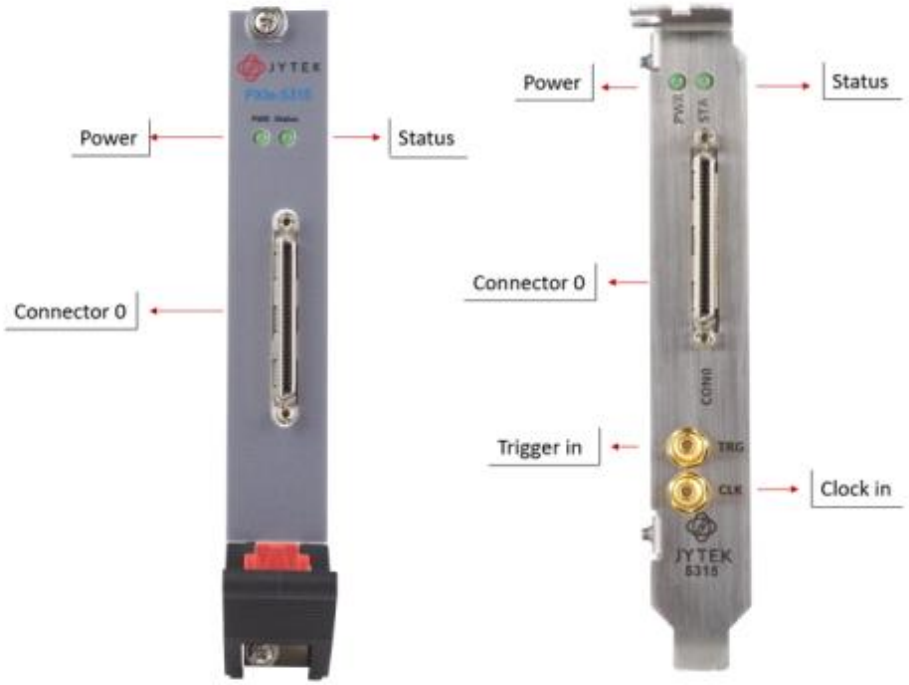

Figure 5 JY5312/5315 Front Panel

JY5312/5315 series are connected to incoming signals by one 68-pin cable for 16 analog input channels and 16 DIO. Table 14 and Table 15 show the pin definition for JY5312/5315 series respectively.

Connector 0			
Pin	**Signal Name**	**Pin**	**Signal Name**
1	PFI0 / P0.0	35	PFI1 / P0.1
2	PFI2 / P1.0	36	PFI3 / P1.1
3	PFI4 / P2.0	37	PFI5 / P2.1
4	PFI6 / P3.0	38	PFI7 / P3.1
5	DGND	39	DGND
6	PFI8 / P4.0	40	PFI9 / P4.1
7	PFI10 / P5.0	41	PFI11 / P5.1
8	PFI12 / P6.0	42	PFI13 / P6.1
9	PFI14 / P7.0	43	PFI15 / P7.1
10	DGND	44	DGND
11	AI7-	45	AI7+
12	AI_GND	46	AI_GND
13	AI15-	47	AI15+
14	AI6-	48	AI6+
15	AI_GND	49	AI_GND
16	AI14-	50	AI14+
17	AI5-	51	AI5+
18	AI_GND	52	AI_GND
19	AI13-	53	AI13+
20	AI4-	54	AI4+
21	AI_GND	55	AI_GND
22	AI12-	56	AI12+
23	AI3-	57	AI3+
24	AI_GND	58	AI_GND
25	AI11-	59	AI11+
26	AI2-	60	AI2+
27	AI_GND	61	AI_GND
28	AI10-	62	AI10+
29	AI1-	63	AI1+
30	AI_GND	64	AI_GND
31	AI9-	65	AI9+
32	AI0-	66	AI0+
33	AI_GND	67	AI_GND
34	AI8-	68	AI8+

Table 14 JY5312/5315 Pin Define

AI_GND	Analog Input Reference Ground
AI<0..15>	Analog Input channel
D_GND	Digital Signal Reference Ground
P<0..7>.<0..1>	Digital I/O Channel
PFI<0..15>	Programmable Function Interface

Table 15 Notes to Legend

3. Software

3.1 System Requirements

JY5312/5315 Modules can be used in a Windows or a Linux operating system.

Microsoft Windows: Windows 7 32/64 bit, Windows 10 32/64 bit.

Linux Kernel Versions: There are many Linux versions. It is not possible JYTEK can support and test our devices under all different Linux versions. JYTEK will at the best support the following Linux versions.

Linux Version
Ubuntu LTS
16.04： 4.4.0-21-generic(desktop/server)
16.04.6：4.15.0-45-generic(desktop) 4.4.0-142-generic(server)
18.04： 4.15.0-20-generic(desktop) 4.15.0-91-generic(server)
18.04.4：5.3.0-28-generic (desktop) 4.15.0-91-generic(server)
Localized Chinese Version
中标麒麟桌面操作系统软件（兆芯版）V7.0（Build61）: 3.10.0-862.9.1.nd7.zx.18.x86_64
中标麒麟高级服务器操作系统软件V7.0U6: 3.10.0-957.el7.x86_64

Table 16 Supported Linux Versions

3.2 System Software

When using JY5312/5315 in the Window environment, you need to install the following software from Microsoft website:

- Microsoft Visual Studio Version 2015 or above.
- .NET Framework version is 4.0 or above.

.NET Framework is coming with Windows 10. For Windows 7, please check .NET Framework version and upgrade to 4.0 or later version.

Given the resources limitation, JYTEK only tested JY5312/5315 with .NET Framework 4.0 with Microsoft Visual Studio 2015. JYTEK relies on Microsoft to maintain the compatibility for the newer versions.

3.3 C# Programming Language

All JYTEK default programming language is Microsoft C#. This is Microsoft recommended programming language in Microsoft Visual Studio and is particularly suitable for the test and measurement applications. C# is also a cross platform programming language.

3.4 JY5312/5315 Hardware Driver

After installing the required application development environment as described above, you need to install the JY5312/5315 hardware driver.

JYTEK hardware driver has two parts:

- the shared common driver kernel software (FirmDrive)
- the specific hardware driver.

Common Driver Kernel Software (FirmDrive): FirmDrive is the JYTEK's kernel software for all hardware products of JYTEK instruments. You need to install the FirmDrive software before using any other JYTEK hardware products. FirmDrive only needs to be installed once. After that, you can install the specific hardware driver.

Specific Hardware Driver: Each JYTEK hardware has a C# specific hardware driver. This driver provides rich and easy-to-use C# interfaces for users to operate various JY5312/5315 function. JYTEK has standardized the ways which JYTEK and other vendor's hardware are used by providing a consistent user interface, using the methods, properties and enumerations in the object-oriented programming environment. Once you get yourself familiar with how one JYTEK DAQ card works, you should be able to know how to use all other DAQ hardware by using the same methods.

Note that this driver does not support cross-process, and if you are using more than one function, it is best to operate in one process.

3.5 Install the SeeSharpTools from JYTEK

To efficiently and effectively use JY5312/5315, you need to install a set of free C# utilities, SeeSharpTools, from JYTEK. The SeeSharpTools offers rich user interface functions you will find convenient in developing your applications. They are also needed to run the examples come with JY5312/5315 hardware. Please register and down load the latest SeeSharpTools from our website, www.jytek.com.

3.6 Running C# Programs in Linux

Most C# written programs in Windows can be run by MonoDevelop development system in a Linux environment. You would develop your C# applications in Windows using Microsoft Visual Studio. Once it is done, run this application in the MonoDevelop environment. This is JYTEK recommended way to run your C# programs in a Linux environment.

If you want to use your own Linux development system other than MonoDevelop, you can do it by using our Linux driver. However, JYTEK does not have the capability to support the Linux applications. JYTEK completely relies upon Microsoft to maintain the cross-platform compatibility between Windows and Linux using MonoDevelop.

4. Operating JY5312/5315

This chapter provides the operation guides for JY5312/5315, including AI and programmable I/O interface, etc.

JYTEK provides extensive examples, on-line help and documentation to assist you to operate the JY5312/5315 board. JYTEK strongly recommends you go through these examples before writing his own application. In many cases, an example can also be a good starting point for a user application.

4.1 Quick Start

After you have installed the driver software and the SeeSharpTools, you are ready to use Microsoft Visual Studio C# to operate JY5312/5315.

If you are already familiar with Microsoft Visual Studio C#, the quickest way to use JY5312/5315 is to go through our extensive examples. We provide source code of our examples. In many cases, you can modify the source code and start to write your applications.

We also provide **Learn by Example** in the following sections. These examples will help you navigate and learn how to use this JY5312/5315.

4.2 Data Acquisition Methods

JY5312/5315 uses a simultaneous method to acquire analog data, meaning there is sixteen ADC chip on the device and each input channel uses individual ADC to capture data. In the simultaneous acquisition mode, you need to configure AI channels and set up some parameters through JY5312/5315 driver software. The most important parameters are *Data Acquisition mode*, *Sample Rate*, *SamplesToAcquire*, *Channel*, and *Analog Input Terminal Type*.

AI Acquisition mode **(***AIMode***)**: JY5312/5315 provides 4 acquisition modes, **Continuous**, **Finite**, **Single Point**, **Record** described in details in Section 4.2.1 to 4.2.4.

SampleRate: How fast multi-channel data are collected per second per channel. Example, if your sample rate is 1000Hz, you acquire two channels of data, you will have 2000 points/second.

SamplesToAcquire: This parameter behaves differently in the different AI acquisition modes. In the continuous acquisition mode, *SamplesToAcquire* is the buffer size used

in the AI acquisition task; in the finite acquisition mode, it is to specify the number of samples to capture.

Channels: how many channels do you want to collect data. You can set up the channels in different orders, for instance 2,3,1,0. The acquired data will be arranged in the way you specified. In this particular case, Channel_Count is 4.

Once the Sample Rate is set, the actual hardware sampling rate is achieved by internal clock or external clock source. The sample clock source is also configured by software. Data acquisition sequence is shown in Figure 6.

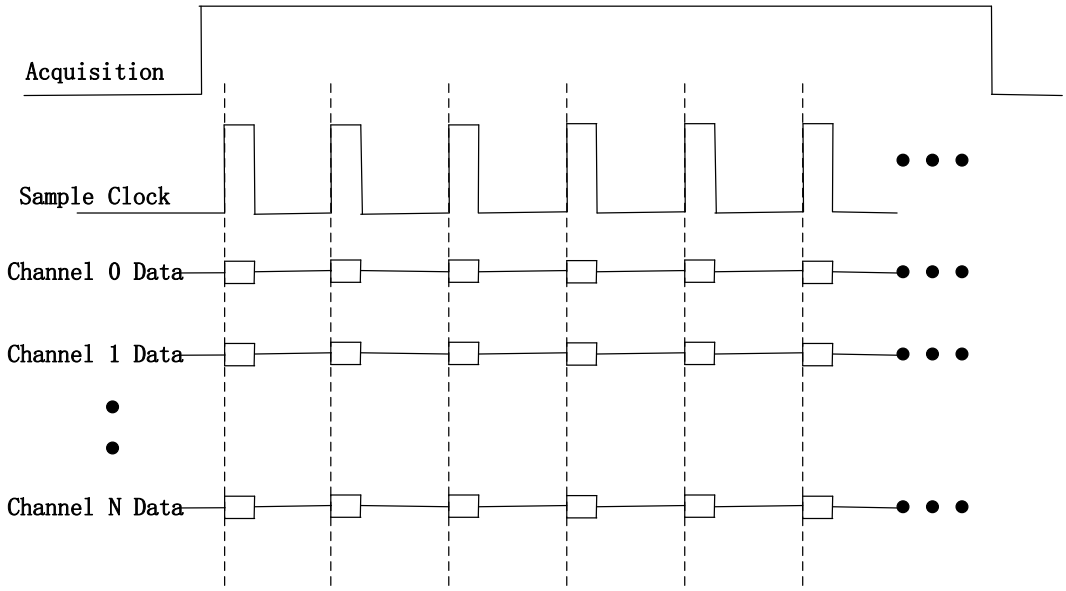

Figure 6 AI Simultaneous Mode Acquisition

4.2.1 Continuous Acquisition

An AI acquisition task will acquire the data continuously until the task is stopped when you start the task in the Continuous acquisition mode. You will need to configure the appropriate buffer size by the parameter, *SamplesToAcquire*, to achieve the best performance of capture and display.

You use the sample program **Analog Input --> Winform AI Continuous** to learn more about Continuous Acquisition

4.2.2 Finite Acquisition

In the Finite Acquisition mode, an AI acquisition task will capture specific number of samples by the parameter, *SamplesToAcquire*.

You use the sample program **Analog Input --> Winform AI Finite** to learn more about Finite Acquisition.

4.2.3 Single Acquisition

In the Single Acquisition mode, it is to capture a single sample for each acquisition.

4.2.4 Record Acquisition

AI Task will continuously capture the data and then save them to a storage disk. During the capturing process, user can preview the captured data randomly when the capturing process is available. The mode is particularly useful for high-speed acquisition and recording applications.

You can use sample program: **Record -->Winform AI Finite Streaming** to learn more about the single point Acquisition.

Learn by Example 4.2

- Connect the two signal source's positive outputs Ch1, Ch2 to JY5312/5315 AI Ch0 positive (AI0+, Pin#66) and AI Ch1 positive (AI1+, Pin#63), two negative terminals to AI Ch0 negative (AI0-, Pin#32) and AI Ch0 negative (AI1-, Pin#29) as shown in Figure 2 and Table 3. (AI0+, AI0-) and (AI1+, AI1-) consist of two channels of DIFF inputs.
- Set the signal source Ch1's output to sinewave (f=1k, Vpp=5v), Ch2's output to squarewave (f=1k, Vpp=3v).
- Open **Analog Input-->Winform AI Continuous MultiChannel**, set the following numbers as shown. This sample program will continuously acquire data from multiple channels.

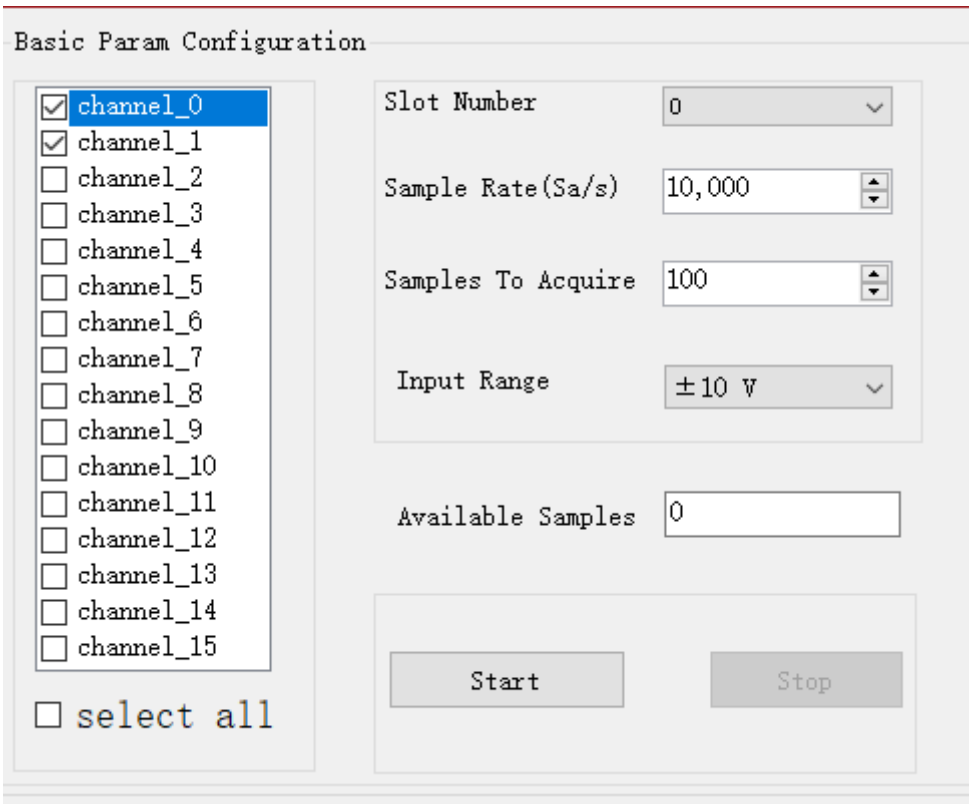

Figure 7 MultiChannel Continuous Parament

- *SampleRate* is set by **Sample Rate**
- **Samples to Acquire** is the samples to be acquired for each channel in one block. The continuous mode will acquire blocks after blocks until **Stop** button is pressed.

■ When **Start** is clicked, the acquisition starts. The result is shown below.

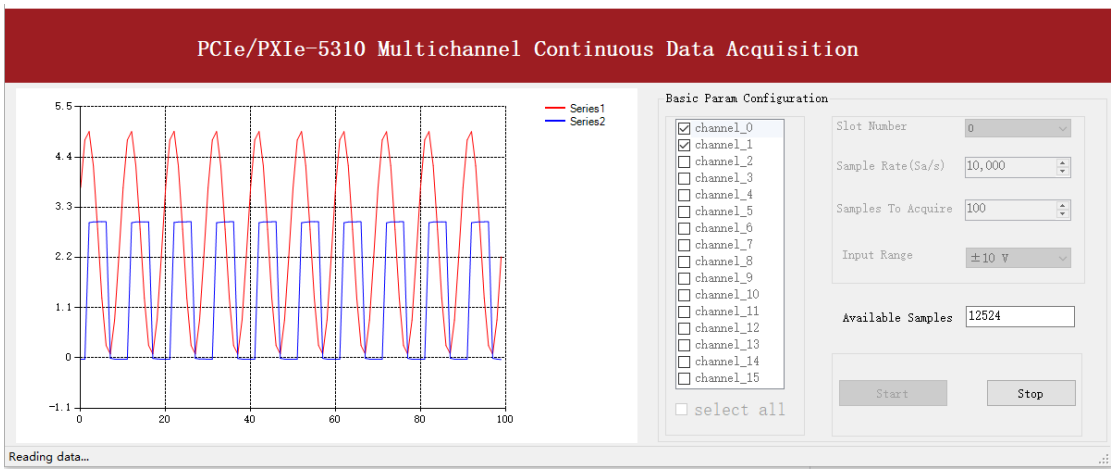

Figure 8 Multichannel Continuous Acquisition

4.3 Analog Input Terminal Type

The JY5312/5315 only provides one analog input terminal type: Differential (DIFF). In the differential mode you can connect ground-referenced signal to the JY5312/5315. Connect positive side of signal to AI+ terminal, negative side of signal to AI- terminal as shown in Figure 9. Please see the provided software examples for more information.

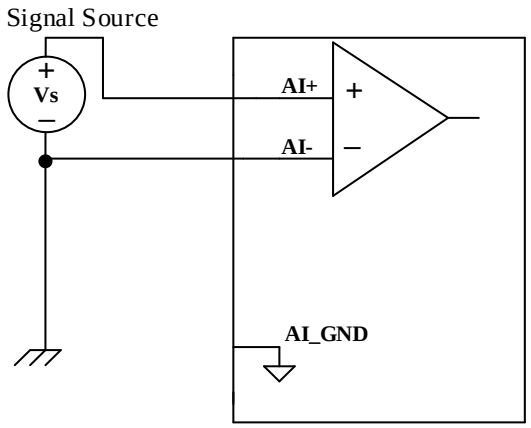

Figure 9 Differential Mode for Grounding Signal

If the measured signal is floating, it is quite often that the common mode voltage will appear. To reduce this effect on the measurement accuracy, a resister can be added as shown in Figure 10. The value of this resister depends on the impedance of the signal source. As a rule of thumb, R should be 1000 times of the signal source output impedance, roughly 10 KΩ to 100 KΩ. At this level, R has very little impact on the measurement.

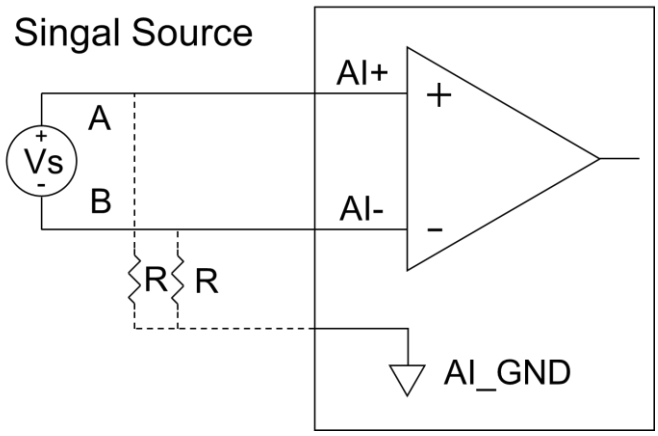

Figure 10 Differential Mode for Floating Signal

4.4 Trigger Source

There are 4 trigger types:

- Immediate trigger
- Software trigger
- analog trigger
- digital trigger

The trigger type is a property and set by driver software. Please find the provided software examples for more information.

4.4.1 Immediate trigger

The module will acquire the signal immediately after executing the AI Task without any trigger condition setting by default.

Learn by Example 4.4.1

- Use the same sample program and connection as in **Learn by Example 4.2.**

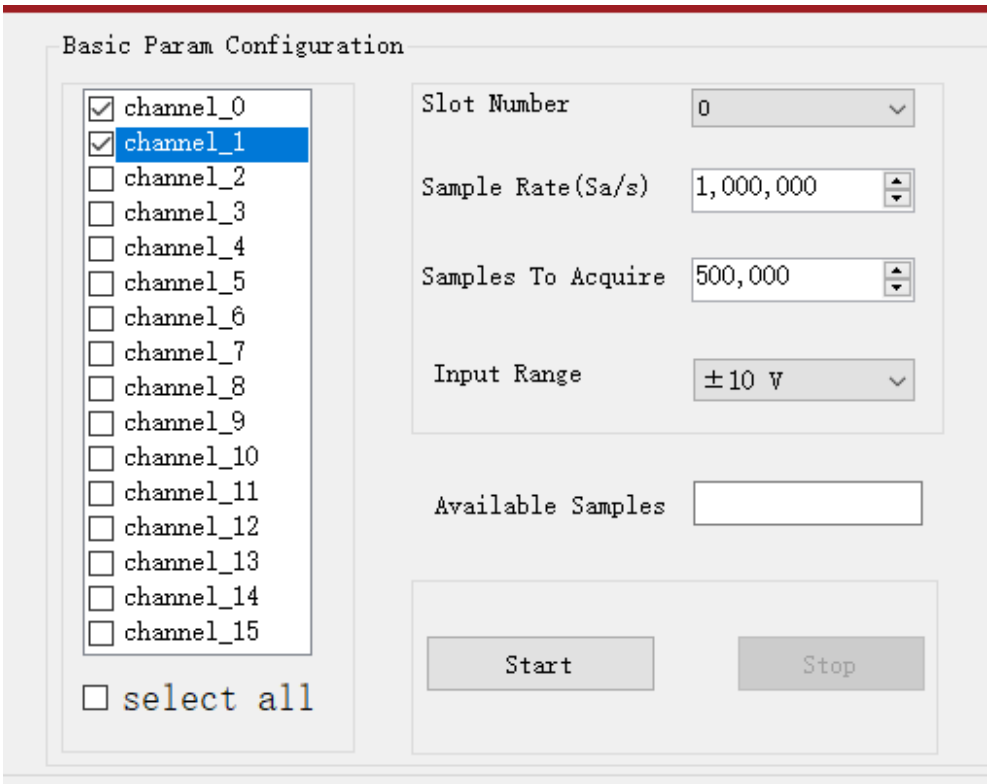

Figure 11 Immediate Trigger Paraments

➢ With *Immediate trigger* you can click **Start** to begin the task instead of sending a trigger signal.

4.4.2 Software Trigger

The analog acquisition task will wait on the software trigger signal in the software trigger mode until receiving a software trigger signal from driver, then AI task will start to acquire the data

Learn by Example 4.4.2

- Connect the signal source's positive terminal Ch1 to JY5312/5315 AI Ch0 positive (AI0+, Pin#66), the negative terminal to AI Ch0 negative (AI0-, Pin#32) as shown in Figure 2 and Table 3. (AI0+, AI0-) consists of a DIFF input.
- Set the signal source Ch1's output to sinewave signal (f=5Hz, Vpp=5v).
- Open **Analog Input-->Winform AI Continuous Soft Trigger**, set the following numbers as shown.

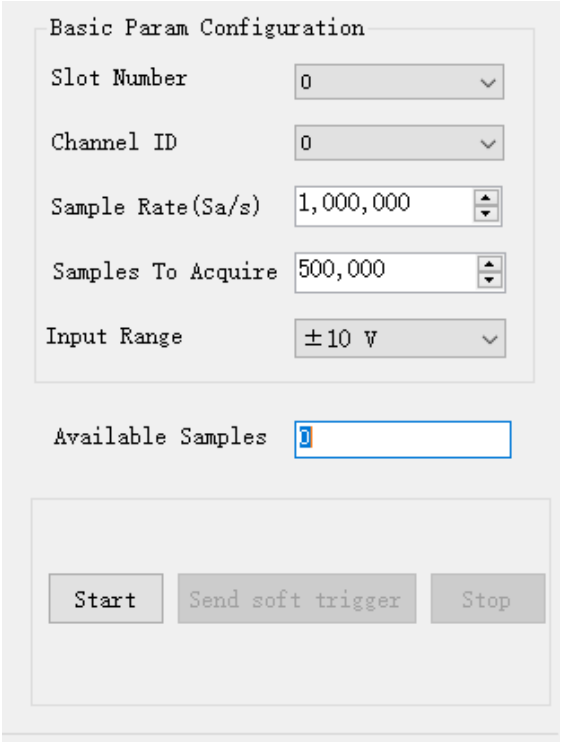

Figure 12 SoftwareTrigger Paraments

➢ Data will not be acquired until there is a positive signal from *Software Trigger* when **Send Soft Trigger** is clicked.
- Click **Start** to run the task.
- After sending the trigger signal, the result will be like this:

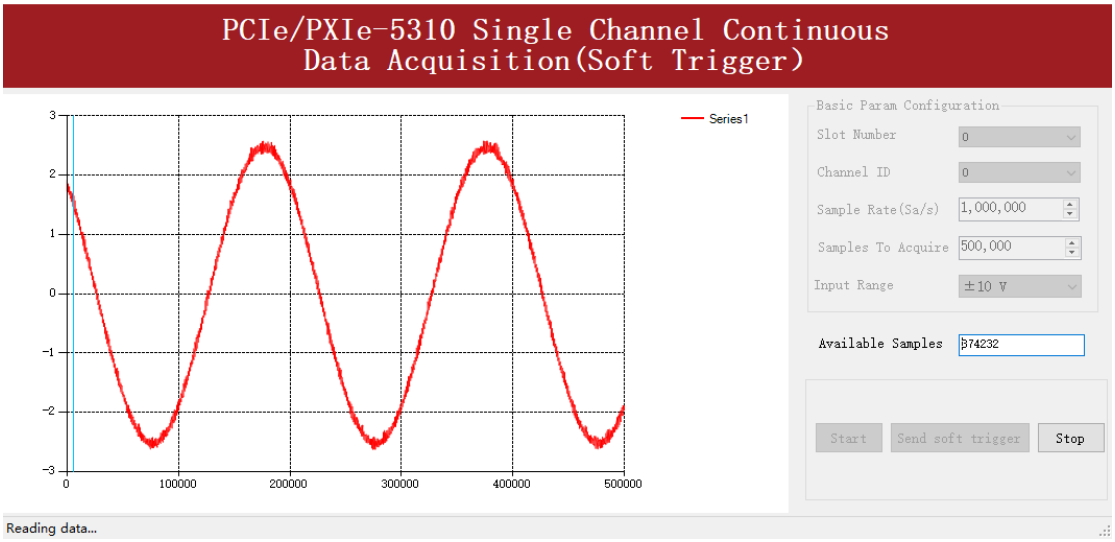

Figure 13 Software trigger Acquisition

4.4.3 External Analog Trigger

User can assign one of measurement channels as the analog trigger source. This module provides three kind of analog trigger: Edge comparator, hysteresis comparator and window comparator. User can select the different analog trigger comparator by setting the parameter "comparator".

Analog trigger threshold can be set arbitrarily in the effective range of the selected channel. When setting the threshold, pay attention to the physical unit currently in use.

Edge comparator

In the Edge comparator, there are two trigger conditions. One is measured value above the specified threshold which is called "Rising Slope Trigger". Another is measured value below the specified threshold which is called "Falling Slope Trigger".

"Rising Slope Trigger": The Edge comparator will output high when the signal go above the threshold. And it will change to low when the signal goes below the threshold as shown in Figure 14.

"Falling Slope Trigger": The Edge comparator will output high when the signal go below the threshold. And it will change to low when the signal goes above the threshold as shown in Figure 15.

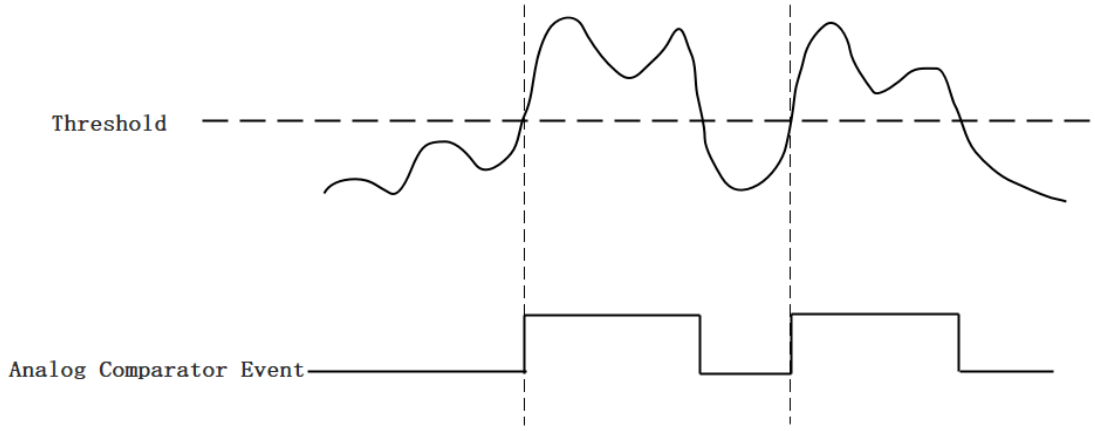

Figure 14 Rising Slope Trigger

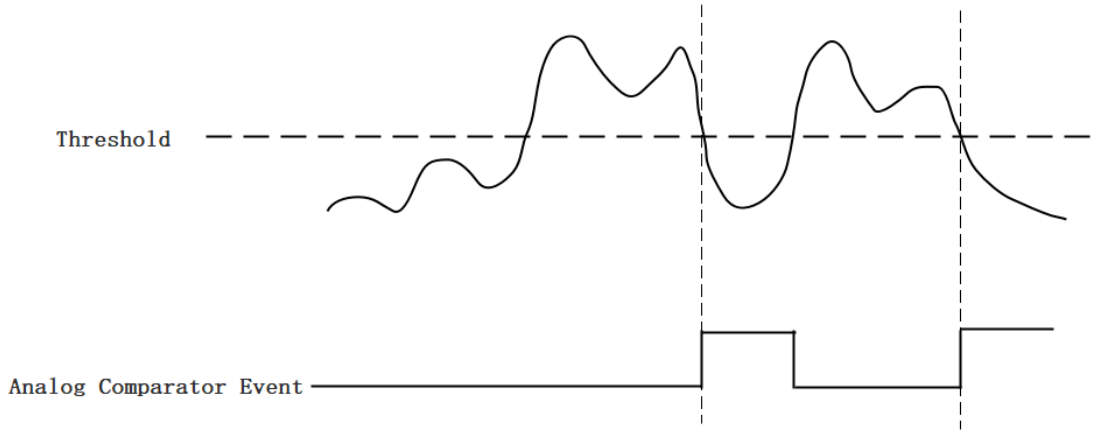

Figure 15 Falling Slope Trigger

Hysteresis comparator

The hysteresis comparator is designed for preventing spurious triggering. User can set hysteresis region by setting high threshold and low threshold. There are two trigger conditions. One is signal passing the hysteresis region from low threshold to high threshold which is called "Hysteresis with Rising Slope Trigger". Another is signal passing the hysteresis region from high threshold to low threshold which is called "Hysteresis with Falling Slope Trigger".

"Hysteresis with Rising Slope Trigger”: The Hysteresis comparator will output high when the signal must first be below the low threshold, then go above the high threshold. It will change to low when the signal goes below the low threshold as shown in Figure 16.

"Hysteresis with Falling Slope Trigger”: The Hysteresis comparator will output high when the signal must first be above the high threshold, then go below the low

threshold. It will change to low when the signal goes above the high threshold as shown in Figure 17.

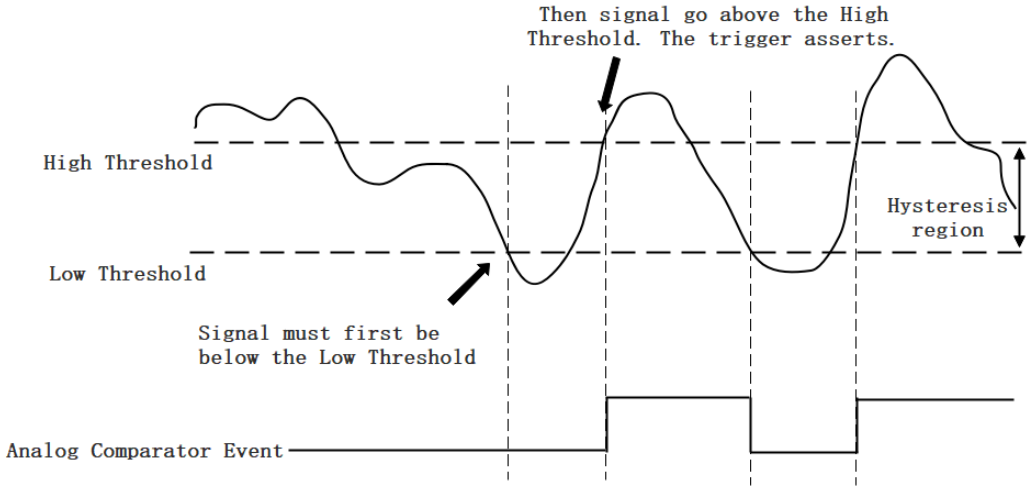

Figure 16 Hysteresis with Rising Slope Trigger

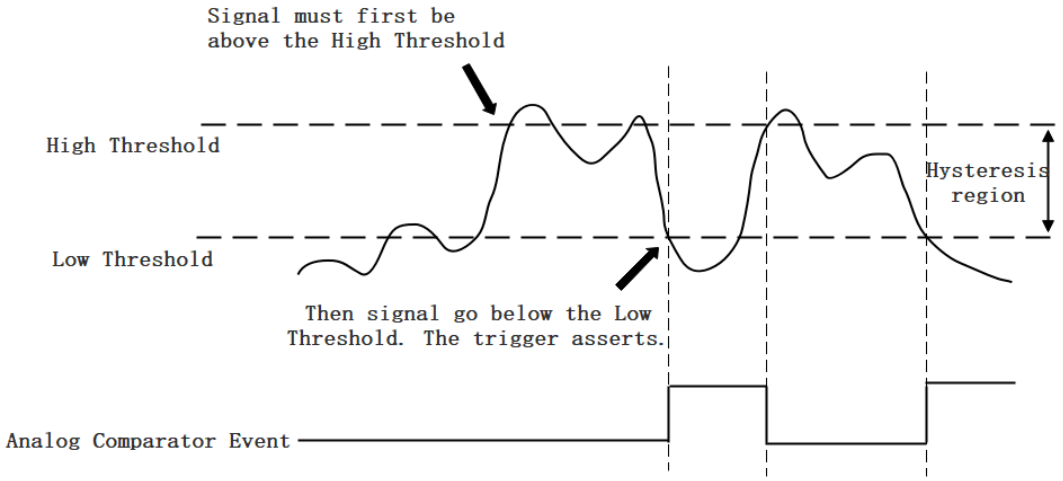

Figure 17 Hysteresis with Falling Slope Trigger

Window comparator

The window comparator is designed to acquire signal from interesting window by setting High Threshold and Low Threshold. There are two trigger conditions. One is acquired the signal inside of the window which is call ed "Entering Window Trigger". Another is acquired the signal outside of the window which is called "Leaving Window Trigger".

"Entering Window Trigger”: The window comparator will output high when the signal enters the window defined by the Low Threshold and High Threshold. And it will output low when the signal leaves the window as shown in Figure 18.

"Leaving Window Trigger”: The window comparator will output high when the signal leaves the window defined by the Low Threshold and High Threshold. And it will output low when the signal enters the window as shown in Figure 19.

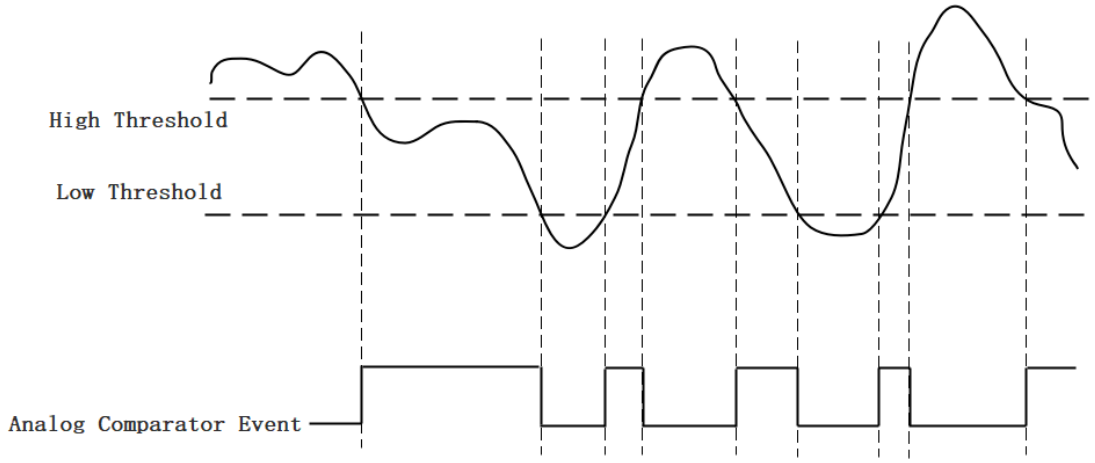

Figure 18 Entering Window Trigger

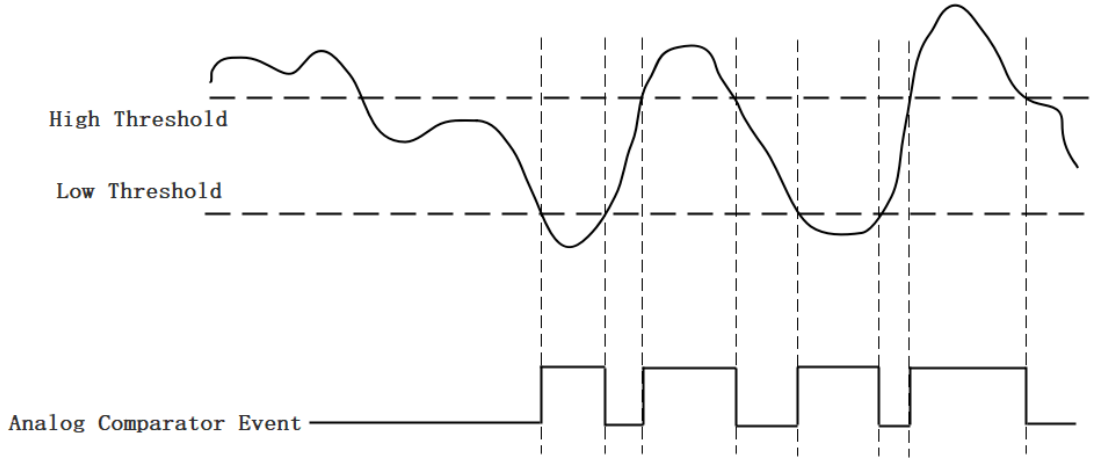

Figure 19 Leaving Window Trigger

Learn by Example 4.4.3

- Connect the signal source’s positive terminal Ch1 to JY5312/5315 AI Ch0 positive (AI0+, Pin#66), the negative terminal to AI Ch0 negative (AI0-, Pin#32) as shown in Figure 2 and Table 3 TB-68 Front Panel for JY5312/5315 Series. (AI0+, AI0-) consists of a DIFF input.
- Set the signal source Ch1’s output to sinewave signal (f=5Hz, Vpp=5v).
- Open **Analog Input-->Winform AI Continuous Analog Trigger**, set the following

numbers as shown.

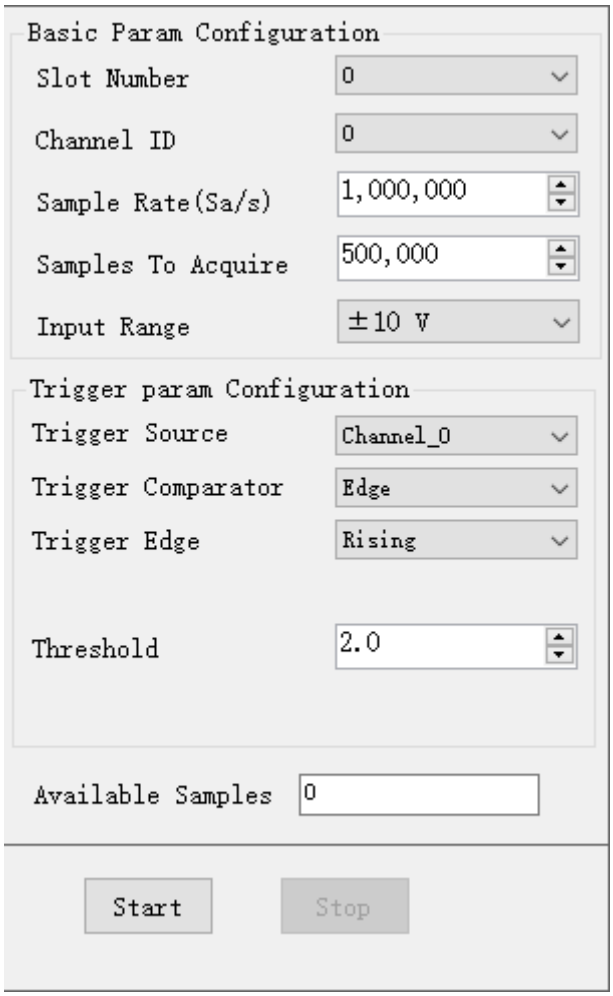

Figure 20 Analog Trigger Paraments

- **Trigger source** can be any channel of JY5312/5315 analog input. Set it to **Channel_0**.
- Comparators of the Analog Trigger are set by **Trigger Comparator.** Set it to **Edge**.
- Trigger edges (rising/falling) are set by **Trigger Edge**. Set it to **Rising**.
- According to the rules of **Edge comparator** mentioned above, the Edge comparator will output high when the signal go above the threshold (2.0V).

■ Click **Start**, a message will appear in the lower left corner:

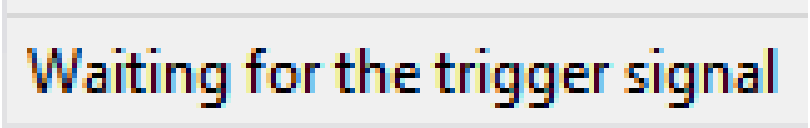

Figure 21 Waiting For Trigger

- This indicates the data acquisition will start only after a triggering event. In this example a trigger signal will occur when the *Edge comparator* is activated.

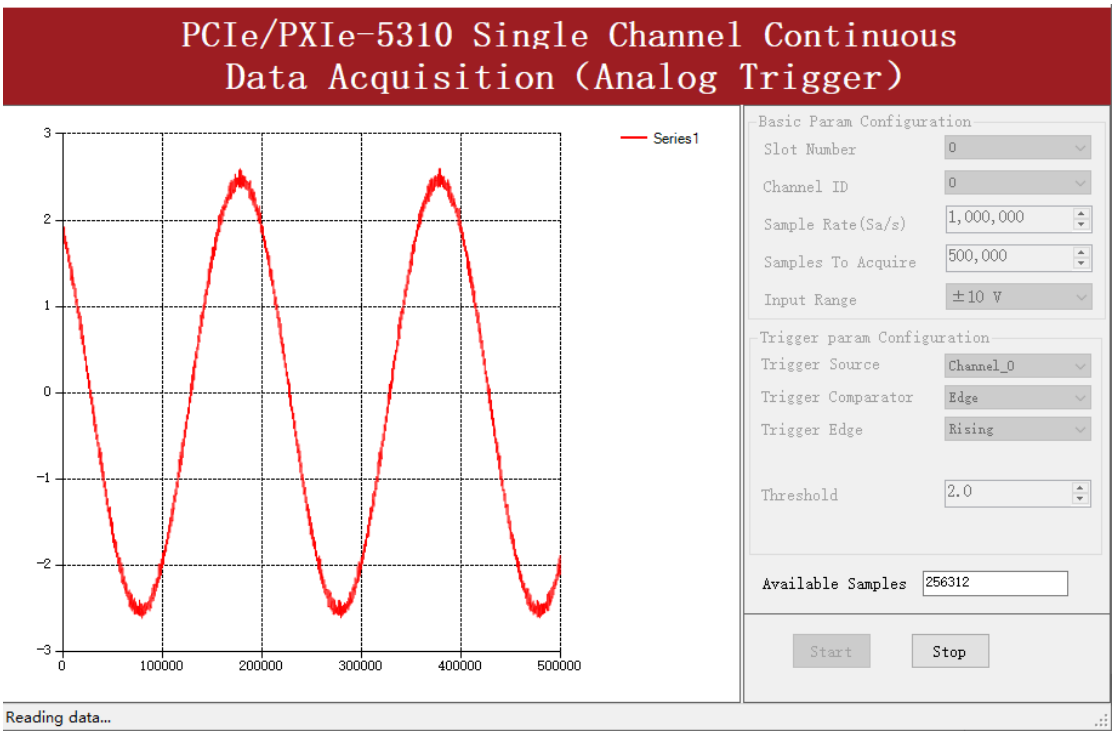

Figure 22 Analog Trigger Acquisition

- The signal starts at 2.0V, which matches the **RisingEdge** mode set before.

4.4.4 External Digital Trigger

The module supports different external digital trigger sources from PXI Trigger bus (PXI_TRIG<0..7>), PXI_STAR and connectors of front panel (PFI). The high pulse width of digital trigger signal must be longer than 20 ns for effective trigger. The module will monitor the signal on digital trigger source and wait for the rising edge or falling edge of digital signal which depending on the set trigger condition, then cause the module to acquire the data as shown in Figure 23.

Figure 23 External Digital Trigger

Learn by Example 4.4.4

- Connect the signal source's two positive terminals Ch1, Ch2 to JY5312/5315 AI Ch0 positive (AI0+, Pin#66) and digital trigger source (PFI0, Pin#1), two negative terminals to AI Ch0 negative (AI0-, Pin#32) and the ground for digital operations (DGND, Pin#5) as shown in Figure 2 and Table 3 TB-68 Front Panel for JY5312/5315 Series. (AI0+, AI0-) consists of a DIFF input. (PFI0, DGND) provides the trigger signal.
- Set the signal source Ch1's output to sinewave signal (f=5Hz, Vpp=5v), Ch2's output to squarewave signal (f=5Hz, V_H=3.3v, V_L=0v).
- Open **Analog Input-->Winform AI Continuous Digital Trigger**, set the following numbers as shown.

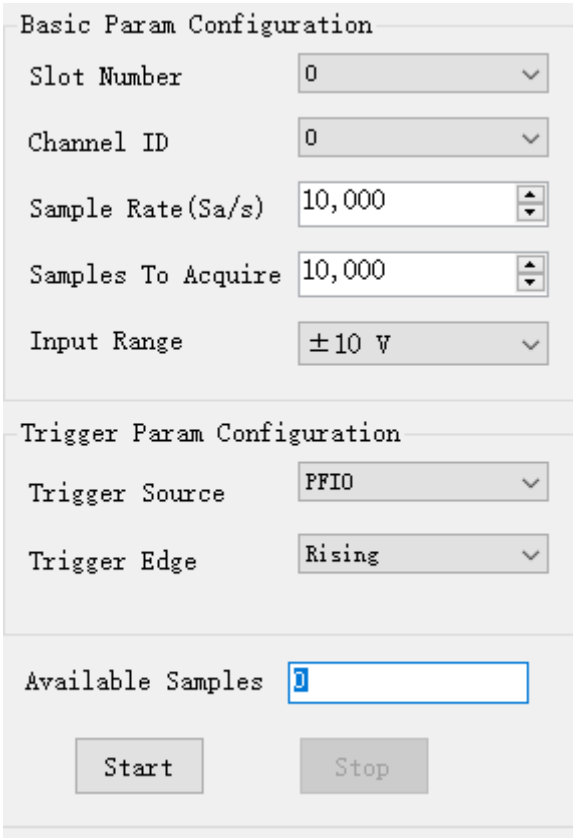

Figure 24 Digital Trigger Paraments

- **Trigger Source** must match the pin on JY5312/5315.
- There are two **Trigger Edge**: **Rising** and **Falling**.
- Click **Start** and the result is shown below:

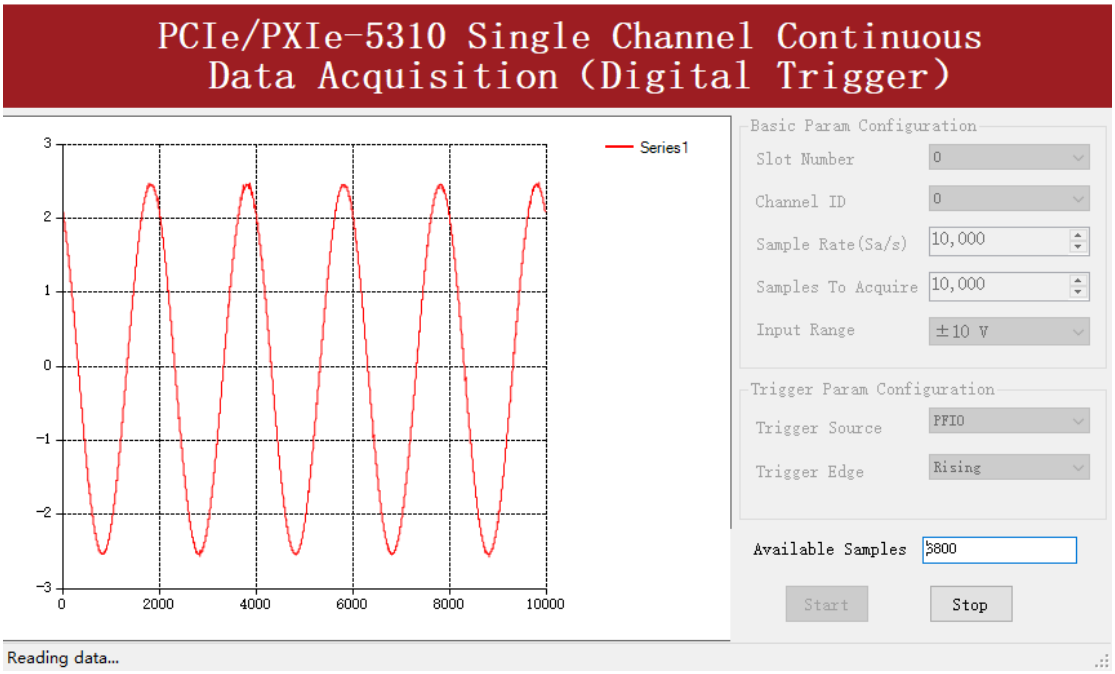

Figure 25 Digital Trigger Acquisition

- Since The squarewave is used for the digital trigger source, when a rising edge of the squarewave occurs, the digital trigger will be activated, and the data acquisition will start.

4.5 Trigger Mode

JY5312/5315 supports several trigger modes: start trigger, reference trigger, and Retrigger. Please see the provided software examples for more information.

4.5.1 Start Trigger

In this mode, data acquisition begins immediately after the trigger. This trigger mode is suitable for continuous acquisition and finite acquisition. As shown in Figure 26. Please see the provided software examples for more information.

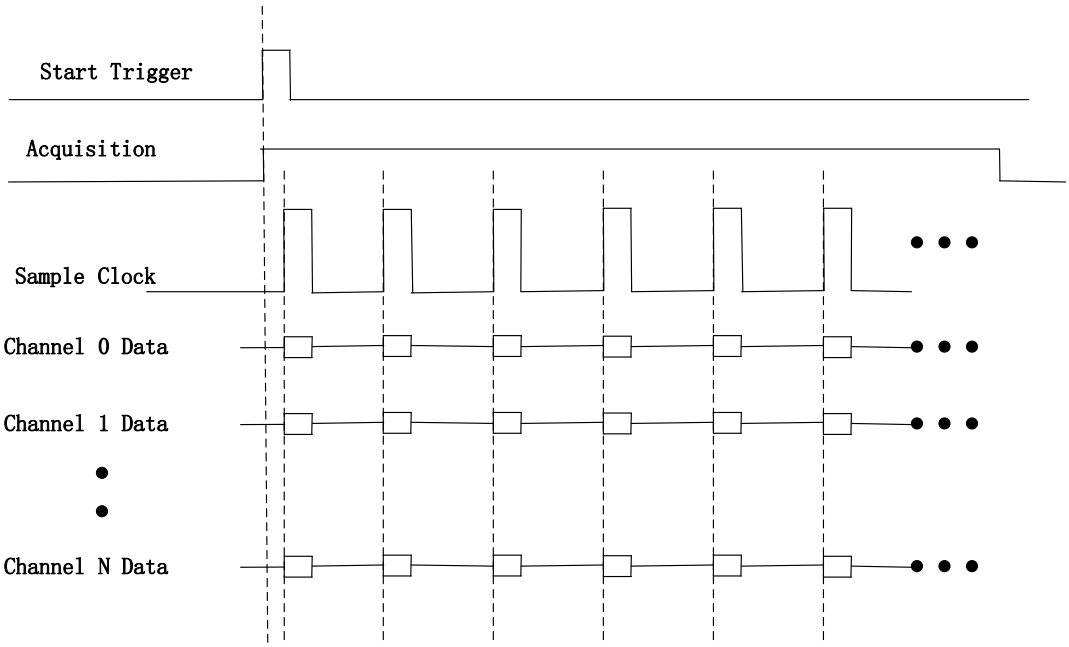

Figure 26 Start Trigger

4.5.2 Reference Trigger

This trigger mode is suitable for finite acquisition. In this mode, user can set the number of pre-trigger samples. The default number of pre-trigger points is 0. First, you need to start the acquisition task and then the acquisition task will return the acquired data when the trigger condition is met. An example is shown below.

Example

- Total samples: 1000;
- Channel Count: 1
- Pre-trigger samples: 10;
- It returns total 1000 samples, 10 samples to be acquired before trigger, 990 samples after trigger.

The acquisition timing is shown in Figure 27. Please see the provided software examples for more information.

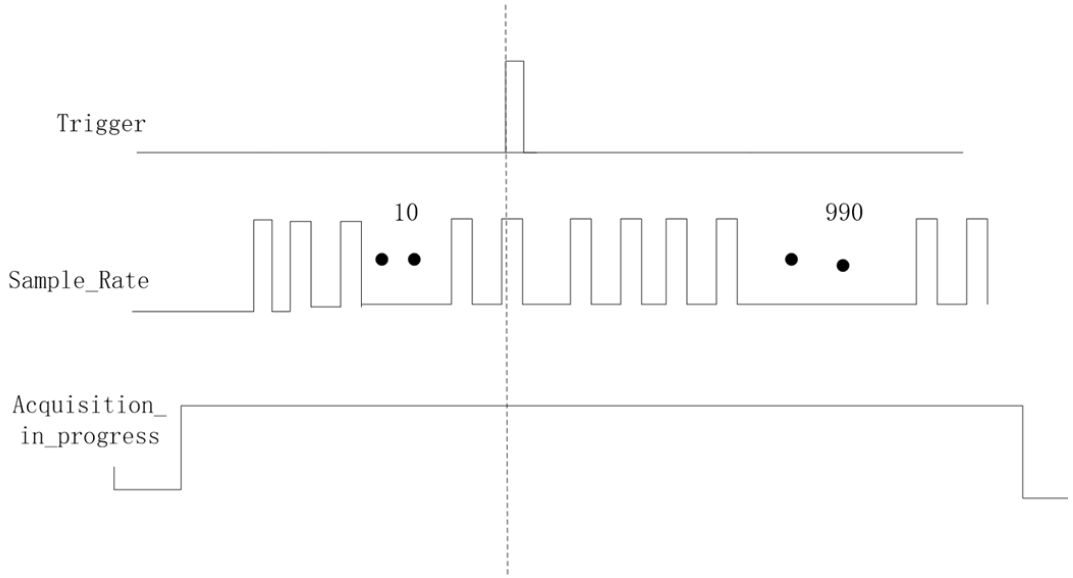

Figure 27 Reference Trigger

4.5.3 ReTrigger

JY5312/5315 series modules support retrigger mode. In the retrigger mode, you can set the number of trigger times and the length of each acquisition. Assuming that the number of trigger times is N and the length of each trigger acquisition is M, the length of all acquisition data is N * M * channelcounts as shown in Figure 28.

When the number of trigger times is - 1, it will wait on trigger infinitely.

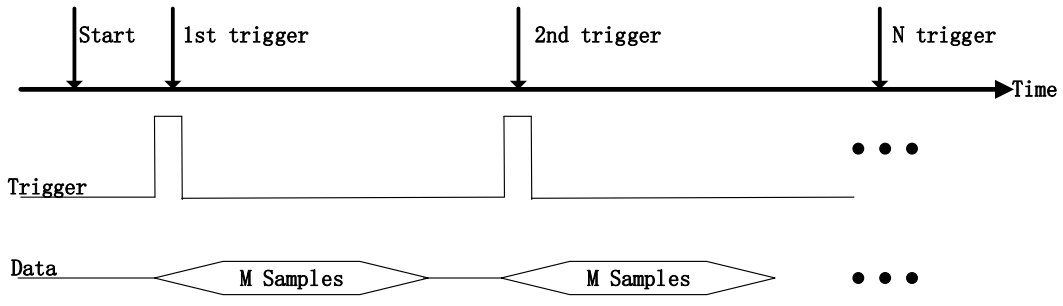

Figure 28 Re-Trigger

Learn by Example 4.5

- Connect the signal source's positive terminal Ch1 to JY5312/5315 AI Ch0 positive (AI0+, Pin#66), the negative terminal to AI Ch0 negative (AI0-, Pin#32) as shown in Figure 2 and Table 3. (AI0+, AI0-) consists of a DIFF input.
- Set the signal source Ch1's output to sinewave signal (f=5Hz, Vpp=5v).
- Open **Analog Input-->Winform AI Finite Analog Trigger**, set the following numbers as shown.

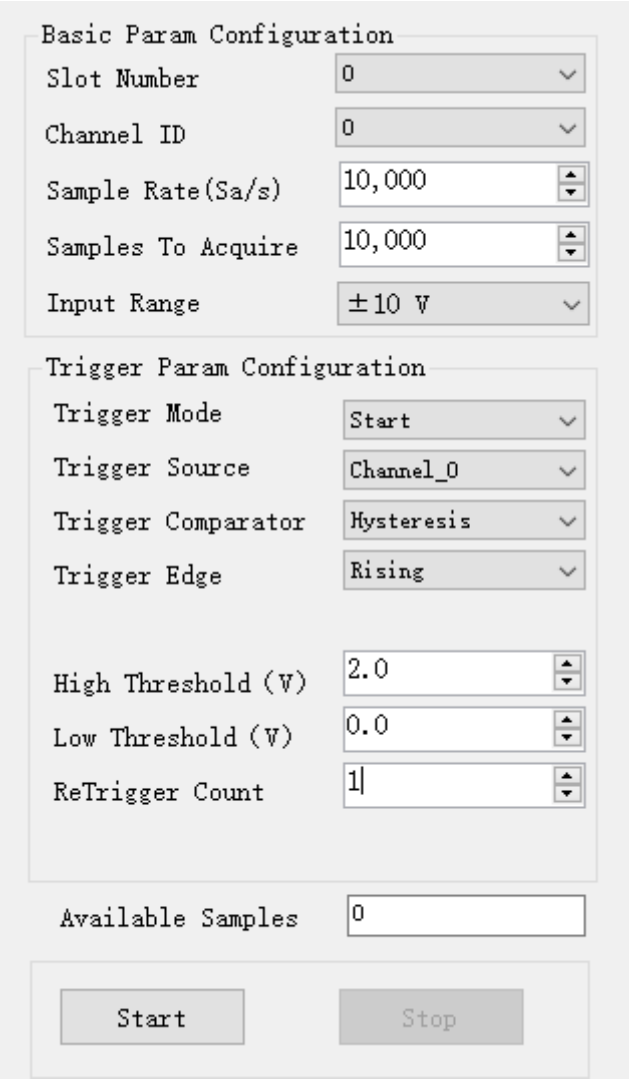

Figure 29 Retrigger Paraments

- You can use three different kinds of triggers in this program as mentioned in this chapter. *Start Trigger* and *Reference Trigger* can be set by **Trigger Mode**. For *ReTrigger* it can be used by changing the numbers in **Retrigger Count**.
- *pretrigger points* is set by **Pretrigger Sample**.

- Now the **Trigger Mode** is "**Start**". Click **Start** to begin the data acquisition, the result is shown below:

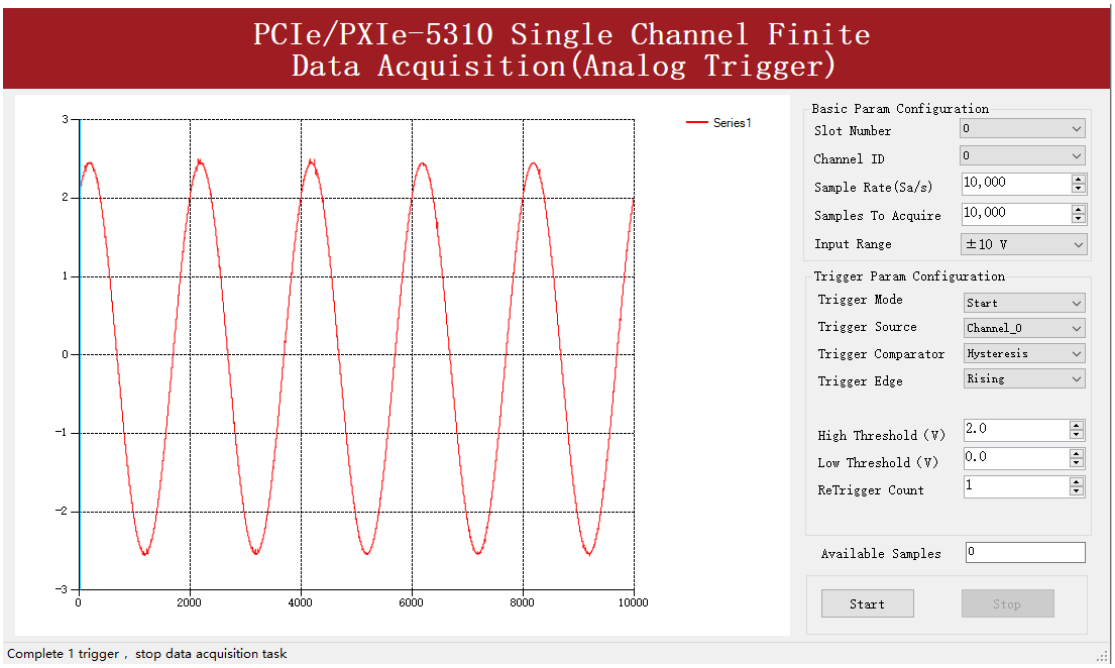

Figure 30 Retrigge rIn Start Trigger Mode

- Now change the **Trigger Mode** to **Reference** mode with **Pretrigger Sample** 1000. A different result is shown below:

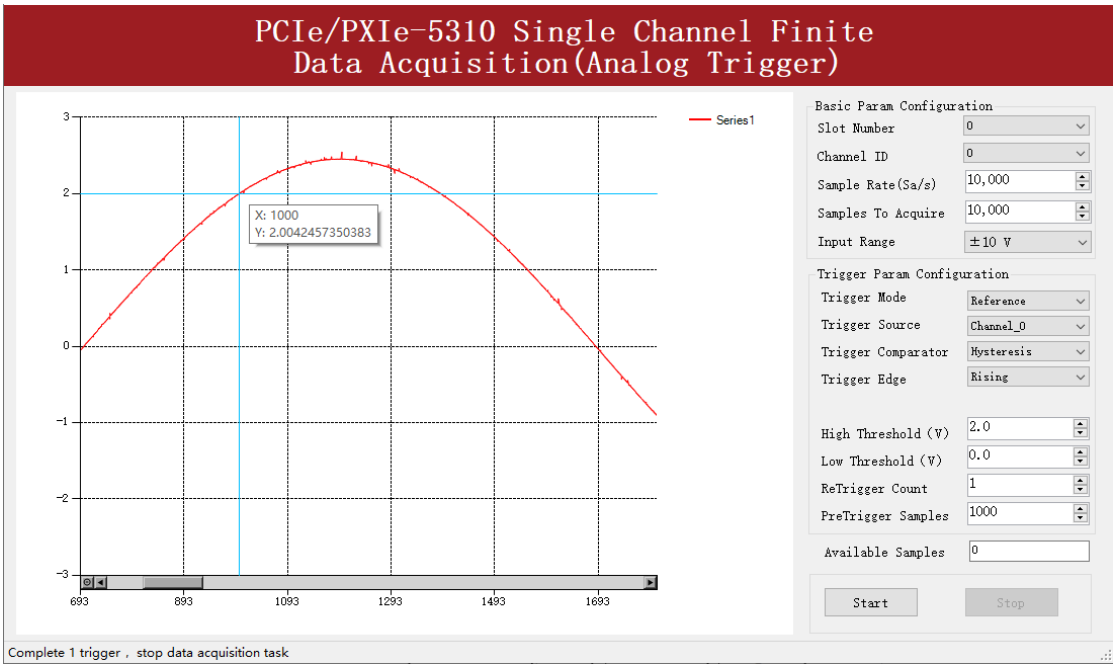

Figure 31 Retrigger in Reference Trigger Mode

- You can see the data acquisition starts with 1000 samples earlier than before due to the change of **Trigger Mode**.

- Now change the mode of trigger to *Retrigger* through giving **Retrigger Count** a number “3”, then click **Start**. A message will appear in the lower left corner: “Complete the n trigger”.

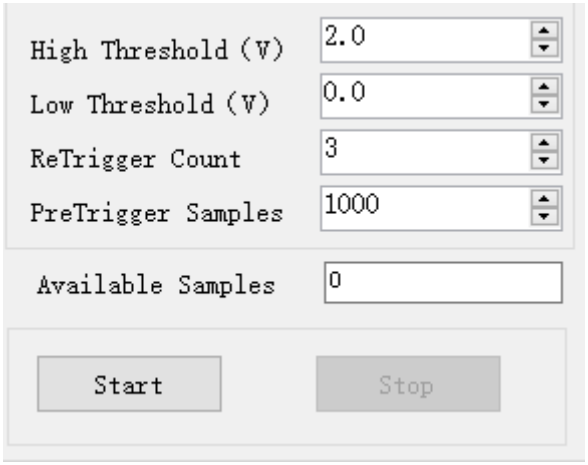

Figure 32 Retrigger Paraments

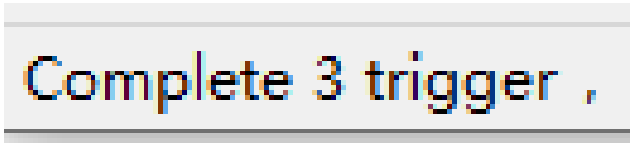

Figure 33 Retrigger Complete State

- It shows the acquisition process through every trigger signal.

4.6 Digital I/O Operations

JY5312/5315 provides powerful programmable digital I/O functions. Please see the provided software examples for more information.

4.6.1 Static DI/DO

Programmable I/O supports static TTL, 8 ports<0..7> with 2 lines which is total 16 channels digital I/O. User can read these I/O information through software polling.

Learn by Example 4.6.1

- In this example JY5312/5315 outputs a digital signal by its DO function and reads it back by its DI function.
- Connect JY5312/5315 Port 0~2's Line 0~1 to Port 3~5's Line 0~1. Connections represented in Pins: (Pin1→Pin4) (Pin2→Pin6) (Pin3→Pin7) (Pin35→Pin38) (Pin36→Pin40) (Pin37→Pin41). JY5312/5315 sends digital signals through Port 3~5 and reads them back from Port 0~2.
- Open the first program **Digital Output-->Winform DO SinglePoint.**
- Select all ports for digital output, Set Line 7,9,11 in High-Level positions, make sure all other lines are in Low-Level positions. Click **Start** to generate the High-Levels as shown.

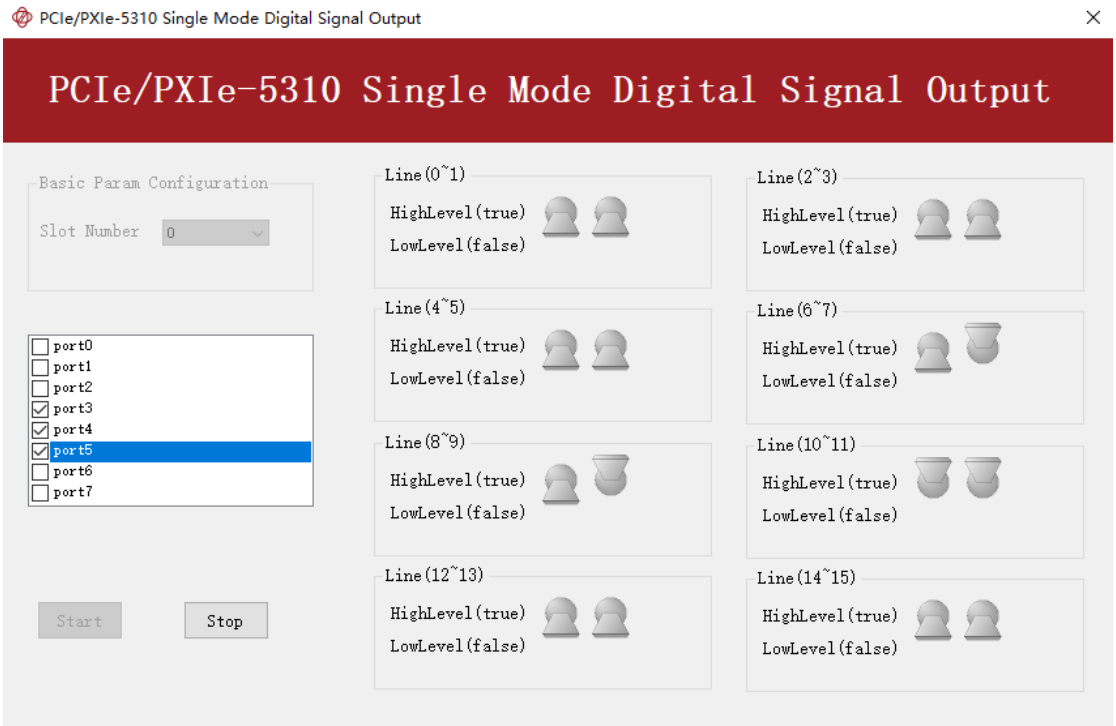

Figure 34 Single Digital Output

- Open the second program **Digital Input-->Winform DI SinglePoint**.
- Select all ports for digital input as shown, and click **Start**. The result is shown below.

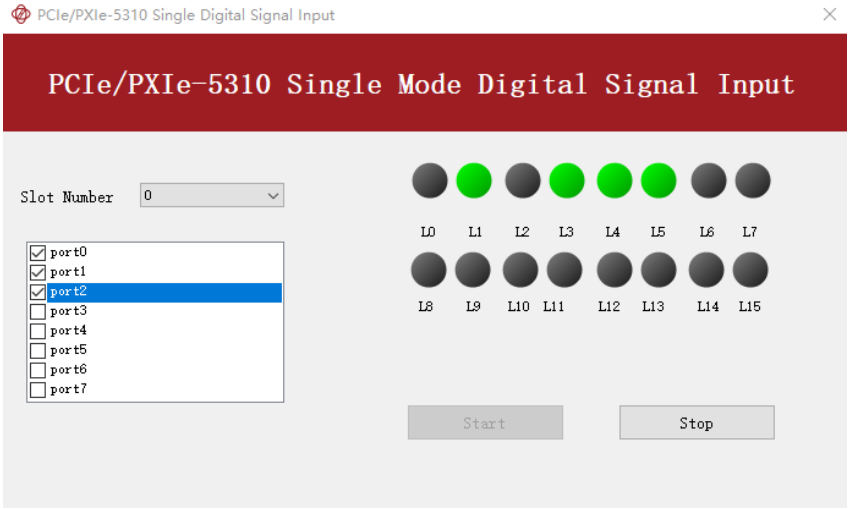

Figure 35 Single Digital Input

➢ The result shows that the digital signals are successfully transferred between Port3~5 and Port 0~2.

4.7 Multi-Devices Synchronization

JY5312/5315 Series modules multi-devices synchronization support two methods : ReferenceClockSynchronization and SampelClockSynchronization

ReferenceClockSynchronization

This method will use 3 signals, Reference clock, Sync Pulse and Triger to achieve data acqusistion simultaneously with multiple modules. First, the master module will notice all of slave modules by routing the trigger signal through PXI trigger bus, PXI_TRIG<0..7> when master module receives trigger. Second, we also need to make sure every module to start the acquisition task in the same time, therefore we could take advange of PXI system which can provide a synchronization pulse, PXIe_SYNC100 to coordinate with the acquisition task of multiple modules.

Third, every module must use the same reference clock to keep pace with each others and user can use PXIe_CLK100 which provides by PXI system as reference clock.

The timing diagram is shown as Figure 36.

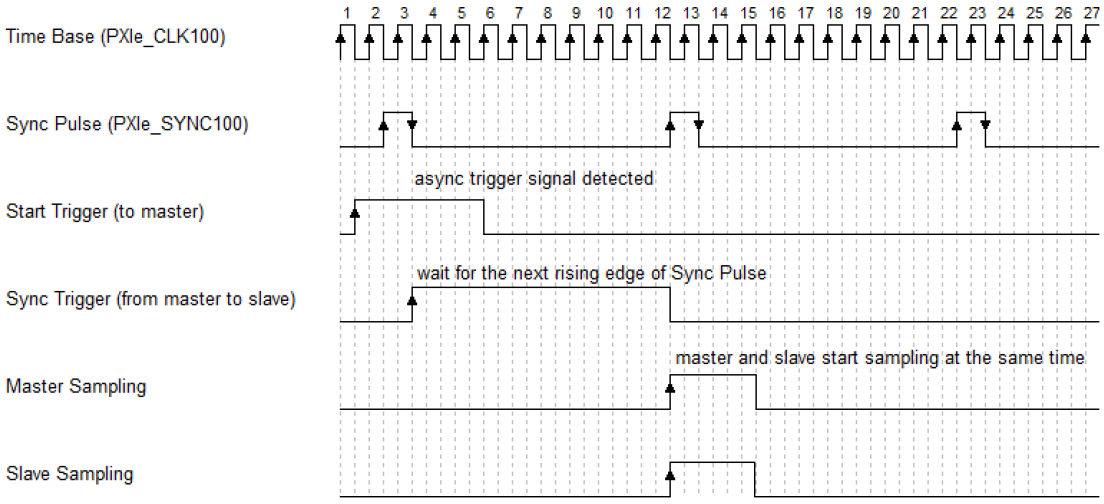

Figure 36 Timing diagram

To enable the multi-card synchronization, configure the board as follows:

1. Set each task on different card as Master or Slave. Only one master is allowed.
2. Set the reference clock source of master card and slave card to PXIe_CLK100.

3. Route trigger signals of all tasks to the same signal terminal, trigger signal will be sent from the master card to all slave cards through this terminal.
4. Route Sync Pulse signals of all tasks to the same signal terminal, Sync Pulse signals will be sent from the master card to all slave cards through this terminal.
5. Start all slave tasks.
6. Start the master task (if digital trigger or software trigger is enabled, you need to wait for the trigger signal to arrive), all the tasks will start to work synchronously on a rising edge of the PXIe_SYNC100 signal.

   Note: The method is only valid for PXIe device.

SampelClockSynchronization

This method will use 2 signals, Sample clock and Triger to achieve data acqusistion simultaneously with multiple modules. First, the master module will routing the Sample clock signal to PXI trigger bus, PXI_TRIG<0..7> , then the slave module must selsect the same PXI trigger bus as the Sample Clock source . Second the master module will notice all of slave modules by routing the trigger signal through PXI trigger bus, PXI_TRIG<0..7> when master module receives trigger.

To enable the multi-card synchronization, configure the board as follows:

1. Set each task on different card as Master or Slave. Only one master is allowed.
2. Export the SampleClock of master card to PXI trigger bus(PXI_TrigN), then the slave cards select the same PXI trigger bus(PXI_TrigN) as external sample clock.
3. Export the trigger signal of master card to PXI trigger bus(PXI_TrigN), then the slave cards select the same PXI trigger bus(PXI_TrigN) as digital trigger source.
4. Start all slave tasks.
5. Start the master task (if digital trigger or software trigger is enabled, you need to wait for the trigger signal to arrive), all the tasks will start to work synchronously.

4.8 System Synchronization Interface（SSI）for PCIe Modules

The synchronization between PCIe modules are handled differently from the PXIe synchronization, it is implemented by the system synchronization interface (SSI). SSI is designed as a bidirectional bus and it can synchronize up to four PCIe modules. One PCIe module is designated as the master module and the other PCIe modules are designated as the slave modules.

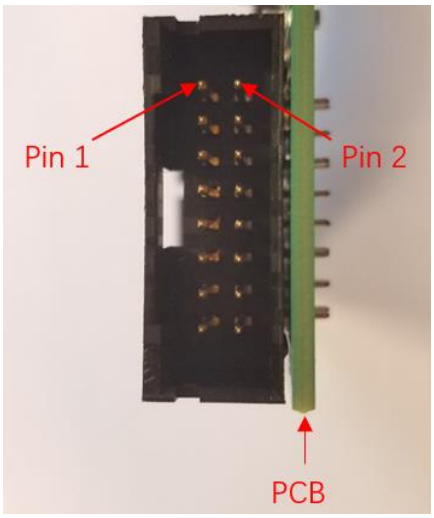

Figure 37 SSI Connector in PCIe-5312/5315

Pin	Signal Name	Signal Name	Pin
1	PXI_TRIG0	GND	2
3	PXI_TRIG1	GND	4
5	PXI_TRIG2	GND	6
7	PXI_TRIG3	GND	8
9	PXI_TRIG4	GND	10
11	PXI_TRIG5	GND	12
13	PXI_TRIG6	GND	14
15	PXI_TRIG7	GND	16

Table 17 SSI Connector Pin Assignment for PCIe-5312/5315

4.9 DIP Switch in PCIe-5312/5315

PCIe-5312/5315 series board has a DIP switch. The card number can be adjusted manually by changing the DIP switch setting, which is used to identify the boards with different slot positions.

For example, if you want to set the card number to 3, you could turn the position 2 and 1 of the DIP switch to the ON position and the orthers to OFF. See below for details.

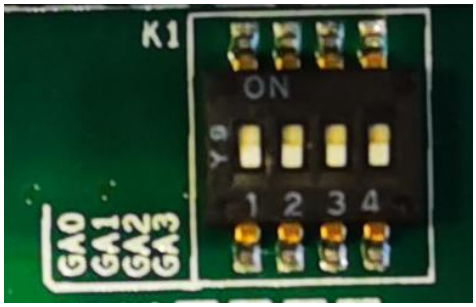

Figure 38 DIP Switch in PCIe-5312/5315

	Position 4 (GA3)	Position 3 (GA2)	Position 2 (GA1)	Position 1 (GA0)
Slot 0	0	0	0	0
Slot 1	0	0	0	1
Slot 2	0	0	1	0
Slot 3	0	0	1	1
Slot 4	0	1	0	0
Slot 5	0	1	0	1
Slot 6	0	1	1	0
Slot 7	0	1	1	1
Slot 8	1	0	0	0
Slot 9	1	0	0	1
Slot 10	1	0	1	0
Slot 11	1	0	1	1
Slot 12	1	1	0	0
Slot 13	1	1	0	1
Slot 14	1	1	1	0
Slot 15	1	1	1	1
Note: OFF=0/ ON=1				

Table 18 Relationship between switch position and slot number

5. Calibration

JY5312/5315 board is precalibrated before the shipment. We recommend you recalibrate your JY5312/5315 board periodically to ensure the measurement accuracy. A commonly accepted practice is one year. If you need to recalibrate your board, please contact JYTEK.

6. About JYTEK

6.1 JYTEK China

Founded in June, 2016, JYTEK China is a leading Chinese test & measurement company, providing complete software and hardware products for the test and measurement industry. The company is a joint venture between Adlink Technologies and a group of experienced professionals form the industry. JYTEK independently develop the software and hardware products and is entirely focused on the Chinese market. Our Shanghai headquarters and production service center have regular stocks to ensure timely supply; we have R&D centers in Xi'an and Chongqing to develop new products; we also have highly trained direct technical sales representatives in Shanghai, Beijing, Tianjin, Xi'an, Chengdu, Nanjing, Wuhan, Haerbin, and Changchun. We also have many partners who provide system level support in various cities.

6.2 JYTEK Korea and JYTEK In Other Countries

JYTEK Korea was the first JYTEK enterprise outside China to promote JYTEK products. Together with Adlink Technologies and JYTEK China, JYTEK is expanding to more countries. Each JYTEK location is an independently owned and operated franchise. It shares JYTEK's philosophy and business approach. Together JYTEK entities promote the JYTEK brand, technology, and products.

6.3 JYTEK Hardware Products

According to JYTEK's agreement with our equity partner Adlink Technologies, JYTEK's hardware is manufactured by the state-of-art manufacturing facility located in Shanghai Zhangjiang Hi-Tech Park. Adlink has over 20 years of the world-class low-volume and high-mix manufacturing expertise with ISO9001-2008, China 3C, UL, ROHS, TL9000, ISO-14001, ISO-13485 certifications. Its 30,000 square meters facilities and three high-speed Panasonic SMT production lines can produce 60,000 pieces boards/month; it also has full supply chain management - planning, sweeping, purchasing, warehousing and distribution. Adlink's manufacturing excellence ensures JYTEK's hardware has word-class manufacturing quality.

One core technical advantage is JYTEK's pursue for the basic and fundamental technology excellence. JYTEK China has developed a unique PCIe, PXIe, USB hardware driver architecture, FirmDrive, upon which many our future hardware will be based.

In addition to our own developed hardware, JYTEK also rebrands Adlink's PXI product lines. In addition, JYTEK has other rebranding agreements to increase our hardware coverage. It is our goal to provide the complete product coverage in PXI and PCI modular instrumentation and data acquisition.

6.4 JYTEK Software Platform

JYTEK has developed a complete software platform, SeeSharp Platform, for the test and measurement applications. We leverage the open sources communities to provide the software tools. Our platform software is also open sourced and is free, thus lowering the cost of tests for our customers. We are the only domestic vendor to offer complete commercial software and hardware tools.

6.5 JYTEK Warranty and Support Services

With our complete software and hardware products, JYTEK is able to provide technical and sales services to wide range of applications and customers. In most cases, our products are backed by a 1-year warranty. For technical consultation, pre-sale and after-sales support, please contact JYTEK of your country.

7. Appendix

7.1 Typical Measurement Error

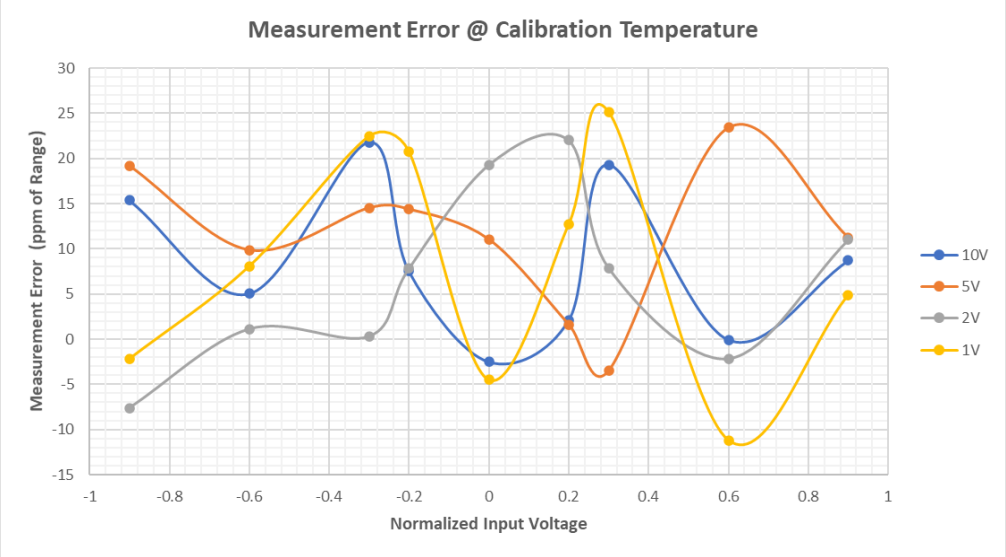

Figure 39 Measurement Error

7.2 System Noise

Range (V)	Random Noise (Test, µVrms)
10	167.0
5	85.9
2	42.9
1	29.1

Table 19 Random Noise

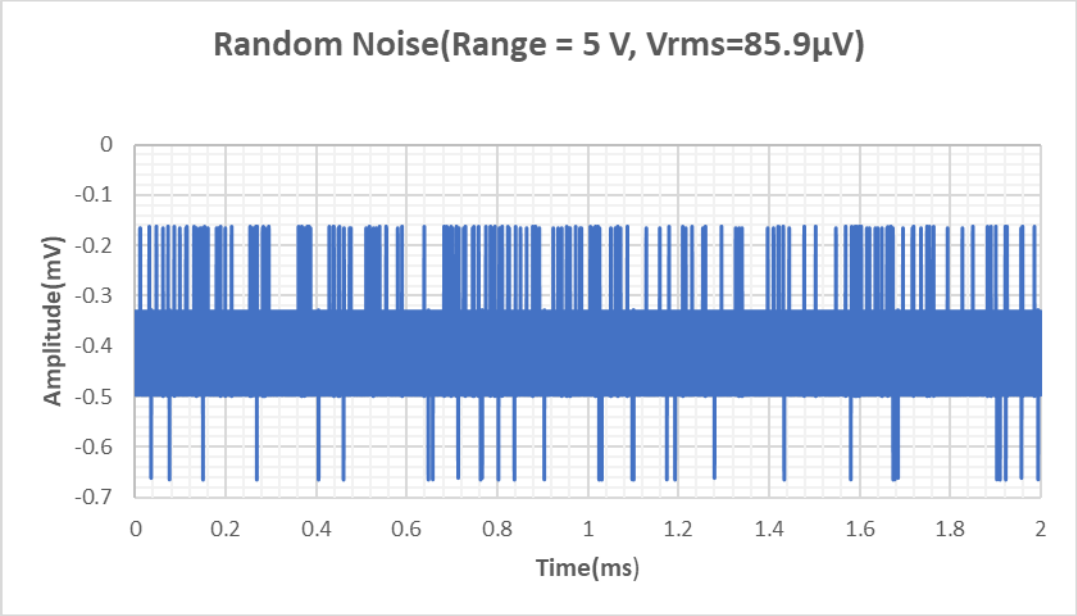

Figure 40 Random Noise

When measuring system noise, the board input bias current must have a return path to its local analog ground. In order to eliminate the bias, it is necessary to connect a ground resistance to the channel, and the resistance should be more than 1MΩ.

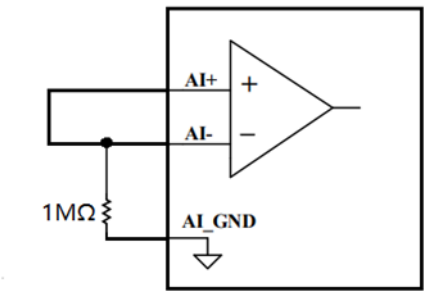

Figure 41 Creating an I_{BIAS} Return Path

7.3 Temperature Drift

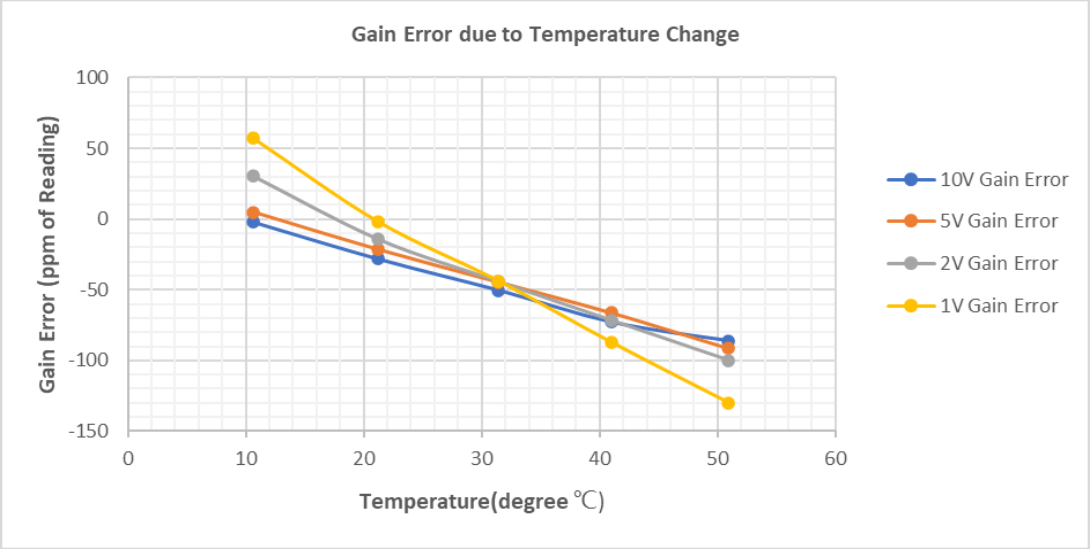

Figure 42 Gain Error due to Temperature Change

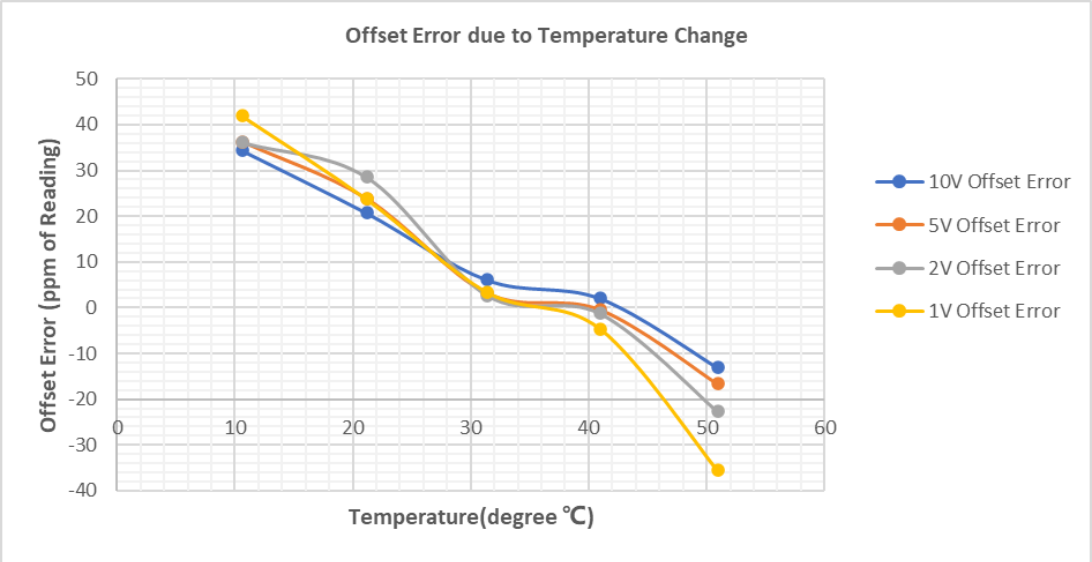

Figure 43 Offset Error due to Temperature Change

8. Statement

The hardware and software products described in this manual are provided by JYTEK China, or JYTEK in short.

This manual provides the product review, quick start, some driver interface explanation for JYTEK JY5312/5315 Series family of multi-function data acquisition boards. The manual is copyrighted by JYTEK.

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While we try to keep this manual up to date, there are factors beyond our control that may affect the accuracy of the manual. Please check the latest manual and product information from our website.

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